MC20902

FPGA Bridge IC

for

MIPI D-PHY Systems
and
LVDS to SLVS Conversion

DATASHEET

Version 1.07

August 2016

Meticom GmbH

Revision History

MC20902		
Version	**Date of Issue**	**Change**
1.00	May 31, 2013	• First Draft
1.01	June 04, 2013	• Table 7, correct data, • Definition for BTA • Minor changes in drawings
1.02	June 07, 2013	• Corrected supply current I_{DD} / I_{DDIO} (Table 3) • Added LP supply current (Table 3)
1.03	August 22, 2013	• Table 3, Table 4: values updated
1.04	March 14, 2014	• BTA description details added
1.05	April 4, 2014	• Package drawing update • Application note added - input to output signal diagram
1.06	August 19, 2014	• Table 4: Propagation delay and delay mismach added • Package dimensions updated • Figure 5: Signal name error corrected
1.07	August 11, 2016	• 'Preliminary' status of data sheet removed • Chapter 6.8 Figure number corrected

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1 General Description

The MC20902 is a 5 Channel, high performance FPGA bridge IC, which converts incoming LVDS high speed and incoming CMOS low speed data streams into a MIPI D-PHY compliant output stream. The MC20902 can also convert an LVDS signal into an SLVS signal.

The MC20902 can be connected to any signal source, for example FPGAs or DSPs.

Data rates can be from 0 Mbps to 2.5 Gbps in HS (High Speed) mode and up to 20 Mbps in LPDT (Low Power Data Transmission) mode.

2 Key Features

- Output is compliant to MIPI D-PHY interfaces using the DSI, CSI-1 and CSI-2 standards
    - HS mode data rate: up to a maximum of 2.5 Gbps
    - LPDT mode data rate: up to 20 Mbps
- BTA supported (Bus Turnaround at Channel A or E)
- Pin Swap possibility
- 5 Channel device
- Conversion of LVDS input to SLVS output
    - LVDS data rate: up to a maximum of 2.5 Gbps
- No additional level shifters needed
- Arbitrary power up sequence
- Available as a bare die
    - RoHS compliant, Pb-free
- Available in a TQLMP-48 package
    - 7mm * 7mm * 0.9mm
    - 0.5mm pitch
    - RoHS compliant, Pb-free

3 Block Diagram

3.1 Block Diagram

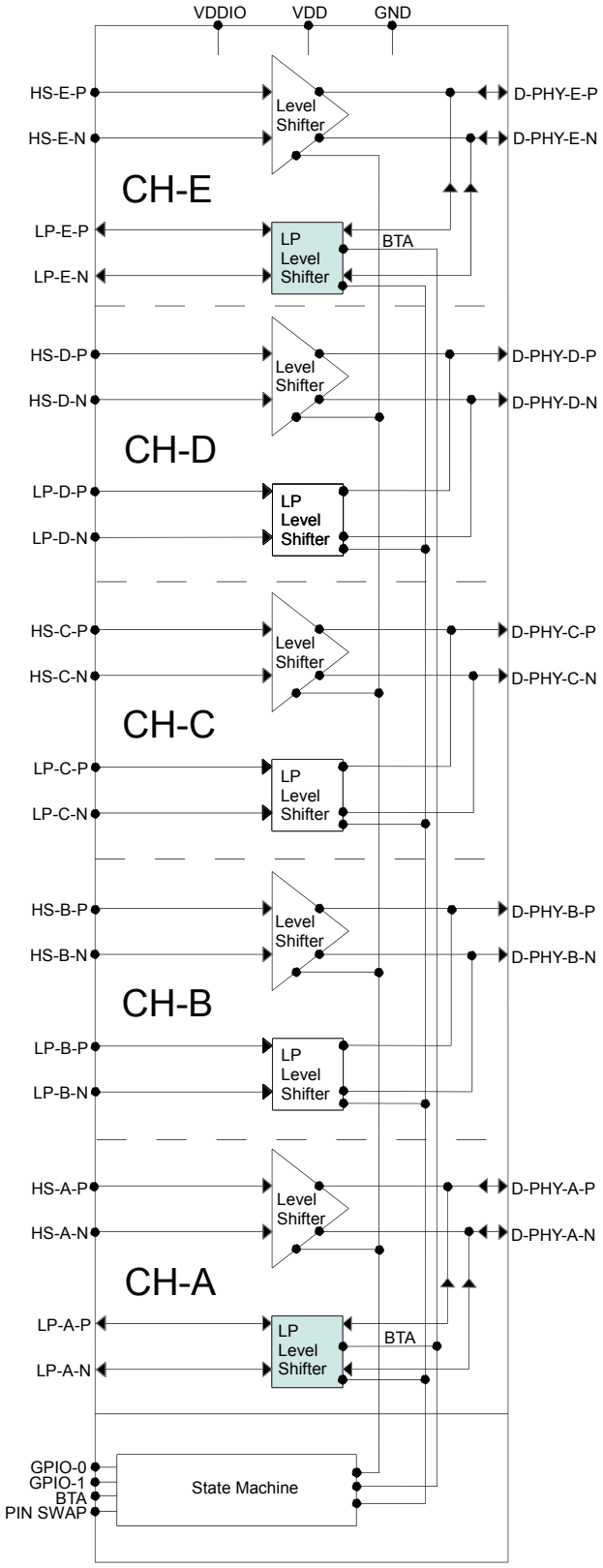


Figure 1: Functional Block Diagram of the MC20902

4 Parametrics

4.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{DDIO}	Supply voltage		-0.5	3.6	V
V_{DD}	Supply voltage		-0.5	2.0	V
T_{STG}	Storage temperature		-55	125	°C
T_J	Junction temperature		-55	125	°C
V_{ESD}	Electrostatic discharge voltage capability	(HBM; 100 pF, 1.5 kΩ)	2.0		kV
$V_{ESD\text{-}Dout}$	Electrostatic discharge voltage capability at differential I/Os	(HBM; 100 pF, 1.5 kΩ)	500		V

Table 1: Absolute Maximum Ratings

Notes:

Absolute Maximum Ratings may not be exceeded to the device without causing permanent damage or degradation. Exposures to these values for extended periods may affect device reliability. If the device is operated beyond the range of Operating Conditions functionality is not guaranteed.

4.2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDIO}	Supply voltage		2.3	2.5	2.7	V
V_{DD}	Supply voltage		1.1	1.2	1.3	V
GND	Ground			0		V
$V_{noise,VDD}$	Maximum allowed supply noise on V_{DD}	see Figure 2			100	mV_{pp}
T_A	Ambient temperature		-40	25	100	ºC

Table 2: Operating Conditions

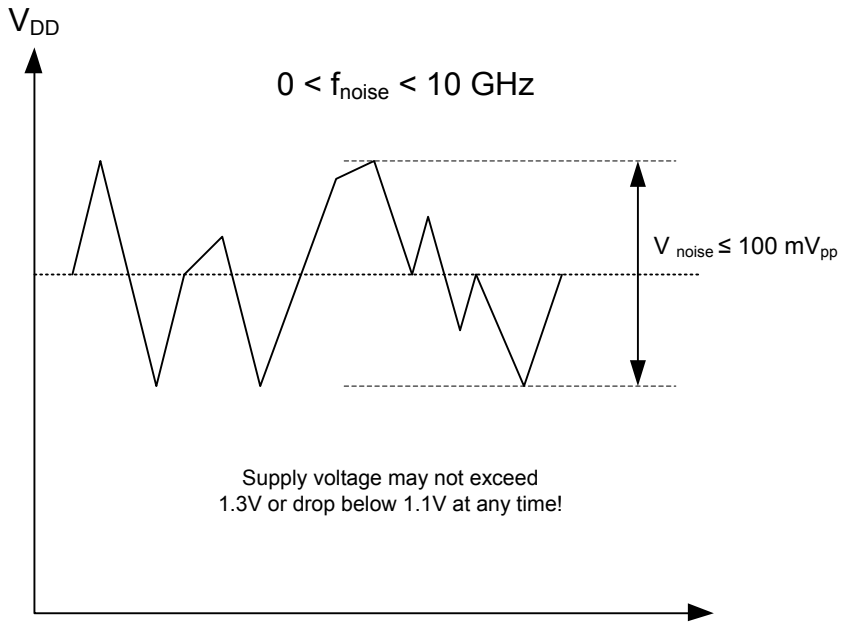


Figure 2: Maximum Allowed Supply Noise on V_{DD}

4.3 DC Characteristics

(At recommended operating conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{DD}	HS mode supply current including SLVS output	D-PHY HS Mode / LVDS to SLVS	10	14.0	18	mA
I_{DDIO}	HS mode supply current	D-PHY HS Mode / LVDS to SLVS	0.6	1.25	1.6	mA
I_{DD}	LP mode supply current		0.5	1.25	1.5	mA
I_{DDIO}	LP mode supply current		0.9	2.0	2.8	mA
Single Ended Input (LP-X-P, LP-X-N, GPIO-0, GPIO-1, BTA, PINSWAP) *)						
V_{IH}	High level input voltage		0.7	V_{DDIO}	V_{DDIO}	V
V_{IL}	Low level input voltage		0		0.5	V
I_{IH}	High level input current	$V_{IN} \geq V_{DDIO} - 0.2$			100	nA
I_{IL}	Low level input current	$V_{IN} \leq 0.2$			100	nA
C_{IN}	Input capacitance	Including package		1	1.5	pF
HS Input (HS-X-P, HS-X-N) *)						
V_{CM-IN}			700	1200	1600	mV
$\|V_{IN-Diff}\|$			70	200	600	mV
Z_{IN}			80	100	125	Ω
Differential Output ($D_{PHY-X-P}$, $D_{PHY-X-N}$) *)						
V_{CM-OUT}	Output common mode voltage	@V_{DD}=1.2V	150	200	250	mV
$\|V_{DO\_DIFF}\|$	Differential output voltage	$\|V_{DPHY-P} - V_{DPHY-N}\|$ @ V_{DD}=1.2V	150	180	250	mV_{pp}
Z_{OD}	Output impedance	Differential	80	100	125	Ω

*) X means the Channels A … E

Table 3: DC Characteristics

4.4 AC Characteristics

(At recommended operating conditions)

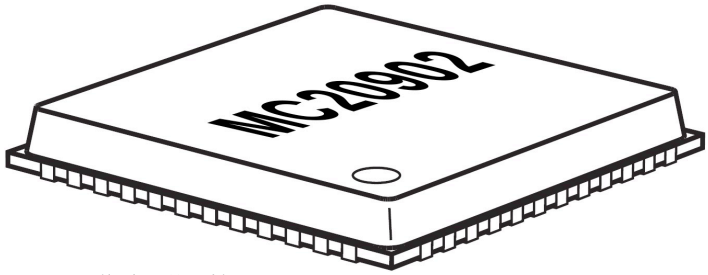
Symbol	Parameter	Condition	Min	Typ	Max	Unit	Notes
HS Input (HS-X-P, HS-X-N) *)							
S_{11}	Input return loss	f <1.04GHz			15	dB	
t_{R,HS_Tx} , $t_{F\ HS\ Tx}$	Input data transition time	20%-80%			0.5	UI	
BR	Supported input data bit rate	for each HS Input	0		2500	Mbps	
LP Input (LP-X-P, LP-X-N, GPIO-0, GPIO-1, BTA, PINSWAP) *)							
BR_{LP}	Maximum LP input bit rate		0		20	Mbps	
Differential Output (D-PHY-X-P, D-PHY-X-N) *)							
BR	Maximum serial output data bit rate	for each PHY Output	2500			Mbps	
t_R, t_F	Output data transition time	20%-80%		90		ps	
S_{22}	Output return loss	f <1.04GHz			15	dB	
		f <625MHz			18	dB	
J_D	Deterministic output jitter	at D_{PHY-P} / D_{PHY-N}			30	ps	
J_R	Generated random output jitter	at D_{PHY-P} / D_{PHY-N}		0.5	0.9	ps_{rms}	
J_{PSRR}	Jitter caused by PSRR	Supply noise @ VDD		1	2	ps/mV	
T_{DEL}	HS propagation delay	HS input to DPHY output	350	600	950	ps	
T_{SKEW}	Propagation delay mismatch	3 sigma mismatch between channels A, B, C, D, E	-	-	50	ps	
$T_{HS-PREPARE}$	$T_{HS-PREPARE}$ (T2out) LP-00		45	60	75	ns	

*) X means the Channels A … E

Table 4: AC Characteristics

5 Package Information

5.1 TQLMP-48 Package



(drawing not to scale)

- Package Type: Thin Quad Leadless Molded Package (TQLMP)
- Package Dimensions: 7.0 x 7.0 x 0.75 mm³
- Pin Pitch: 0.5 mm

5.2 Pin Description

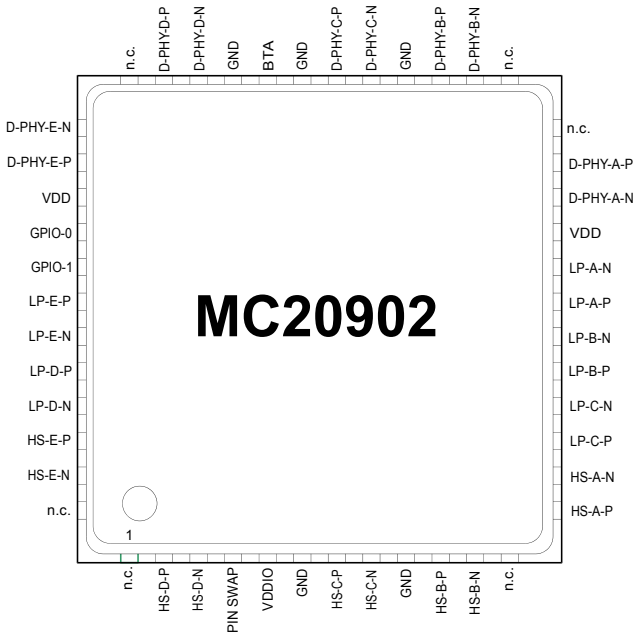
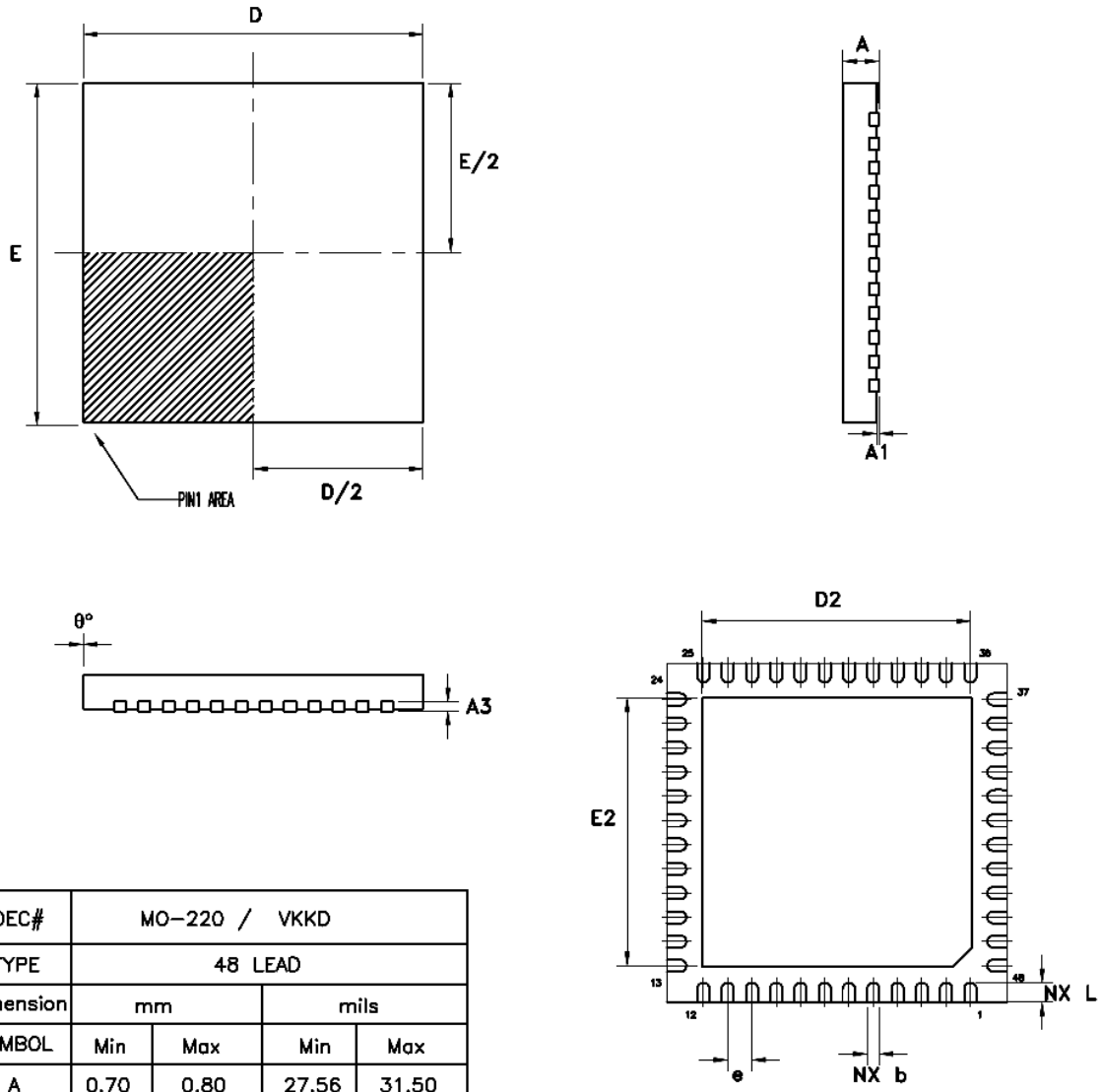


Figure 3: Pin Assignment MC20902

Pin Name	Pin No.	I/O	Type	Description
VDD	21, 39	P	Supply	Supply voltage for internal logic and SLVS output drivers
VDDIO	5	P	Supply	Supply voltage for internal level shifters and LVDS input stage
GND	6, 9, 28, 31, 33	-	-	Global ground
D-PHY-A-P	23	I/O	SLVS/CMOS	MIPI D-PHY compliant positive output or SLVS positive output, channel A, input for BTA
D-PHY-A-N	22	I/O	SLVS/CMOS	MIPI D-PHY compliant negative output or SLVS negative output, channel A, input for BTA
HS-A-P	13	I	LVDS	Positive LVDS high speed input, channel A
HS-A-N	14	I	LVDS	Negative LVDS high speed input, channel A
LP-A-P	19	I/O	CMOS	Positive CMOS low power data input, channel A, output for BTA
LP-A-N	20	I/O	CMOS	Negative CMOS low power data input, channel A, output for BTA
D-PHY-B-P	27	O	SLVS/CMOS	MIPI D-PHY compliant positive output or SLVS positive output, channel B
D-PHY-B-N	26	O	SLVS/CMOS	MIPI D-PHY compliant negative output or SLVS negative output, channel B
HS-B-P	10	I	LVDS	Positive LVDS high speed input, channel B
HS-B-N	11	I	LVDS	Negative LVDS high speed input, channel B
LP-B-P	17	I	CMOS	Positive CMOS low power data input, channel B
LP-B-N	18	I	CMOS	Negative CMOS low power data input, channel B
D-PHY-C-P	30	O	SLVS/CMOS	MIPI D-PHY compliant positive output or SLVS positive output, channel C
D-PHY-C-N	29	O	SLVS/CMOS	MIPI D-PHY compliant negative output or SLVS negative output, channel C
HS-C-P	7	I	LVDS	Positive LVDS high speed input, channel C
HS-C-N	8	I	LVDS	Negative LVDS high speed input, channel C
LP-C-P	15	I	CMOS	Positive CMOS low power data input, channel C
LP-C-N	16	I	CMOS	Negative CMOS low power data input, channel C
D-PHY-D-P	35	O	SLVS/CMOS	MIPI D-PHY compliant positive output or SLVS positive output, channel D
D-PHY-D-N	34	O	SLVS/CMOS	MIPI D-PHY compliant negative output or SLVS negative output, channel D
HS-D-P	2	I	LVDS	Positive LVDS high speed input, channel D
HS-D-N	3	I	LVDS	Negative LVDS high speed input, channel D
LP-D-P	44	I	CMOS	Positive CMOS low power data input, channel D
LP-D-N	45	I	CMOS	Negative CMOS low power data input, channel D
D-PHY-E-P	38	I/O	SLVS/CMOS	MIPI D-PHY compliant positive output or SLVS positive output, channel E, input for BTA
D-PHY-E-N	37	I/O	SLVS/CMOS	MIPI D-PHY compliant negative output or SLVS negative output, channel E, input for BTA
HS-E-P	46	I	LVDS	Positive LVDS high speed input, channel E
HS-E-N	47	I	LVDS	Negative LVDS high speed input, channel E
LP-E-P	42	I/O	CMOS	Positive CMOS low power data input, channel E, output for BTA
LP-E-N	43	I/O	CMOS	Negative CMOS low power data input, channel E, output for BTA
GPIO-0	40	I	CMOS	General purpose configuration input 0
GPIO-1	41	I	CMOS	General purpose configuration input 1
BTA	32	I	CMOS	Bus turnaround control pin
PINSWAP	4	I	CMOS	Pin swap function control pin
N.C.	1, 12, 24, 25, 36, 48	-	-	Do not connect
Thermal Pad	-	-	-	Thermal Pad may be connected to GND or left floating (n.c.)

Table 5: Pin Description

5.3 Package Information



JEDEC#	MO-220 / VKKD			
TYPE	48 LEAD			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.70	0.80	27.56	31.50
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	6.9	7.1	271.65	279.53
E	6.9	7.1	271.65	279.53
D2	5.5	5.6	216.54	220.47
E2	5.5	5.6	216.54	220.47
e	0.5 BSC		19.69 BSC	
NX b	0.20	0.30	7.87	11.81
NX L	0.35	0.45	13.78	17.72
θ°	0°	4°	0°	4°
ND	12			
NE	12			

NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
   DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

Figure 4: Mechanical Dimensions TQLMP-48

6 Application Notes

6.1 Application Overview

MC20902 can be used together with D-PHY sink (such as a display) as shown. It can take standard LVDS and CMOS signals from an FPGA or DSP and converts them into D-PHY compliant output streams, which can then be fed directly into a D-PHY compliant display.

The diagram also shows the MC20901, which performs the reverse function of the MC20902.

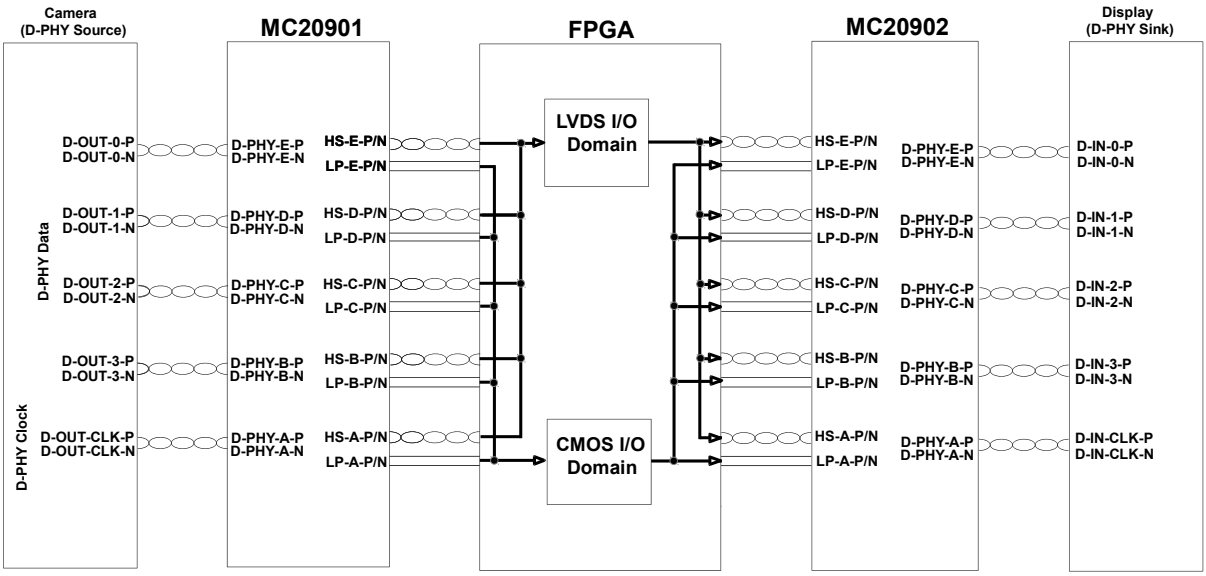


Figure 5: Application Diagram

6.2 FPGA to D-PHY Bridge Application

In this example one D-PHY clock lane and four D-PHY data lanes in regular configuration are shown.

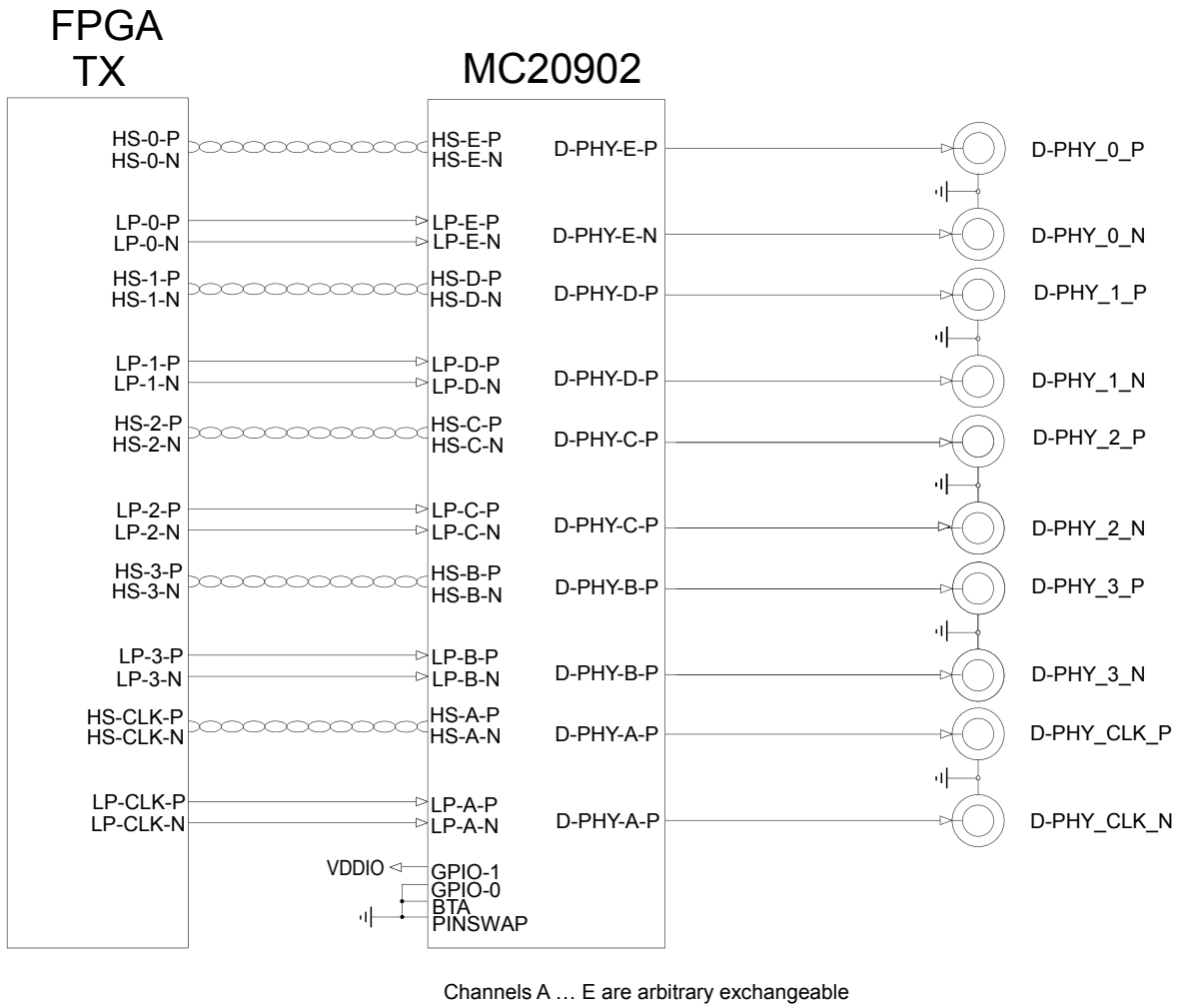
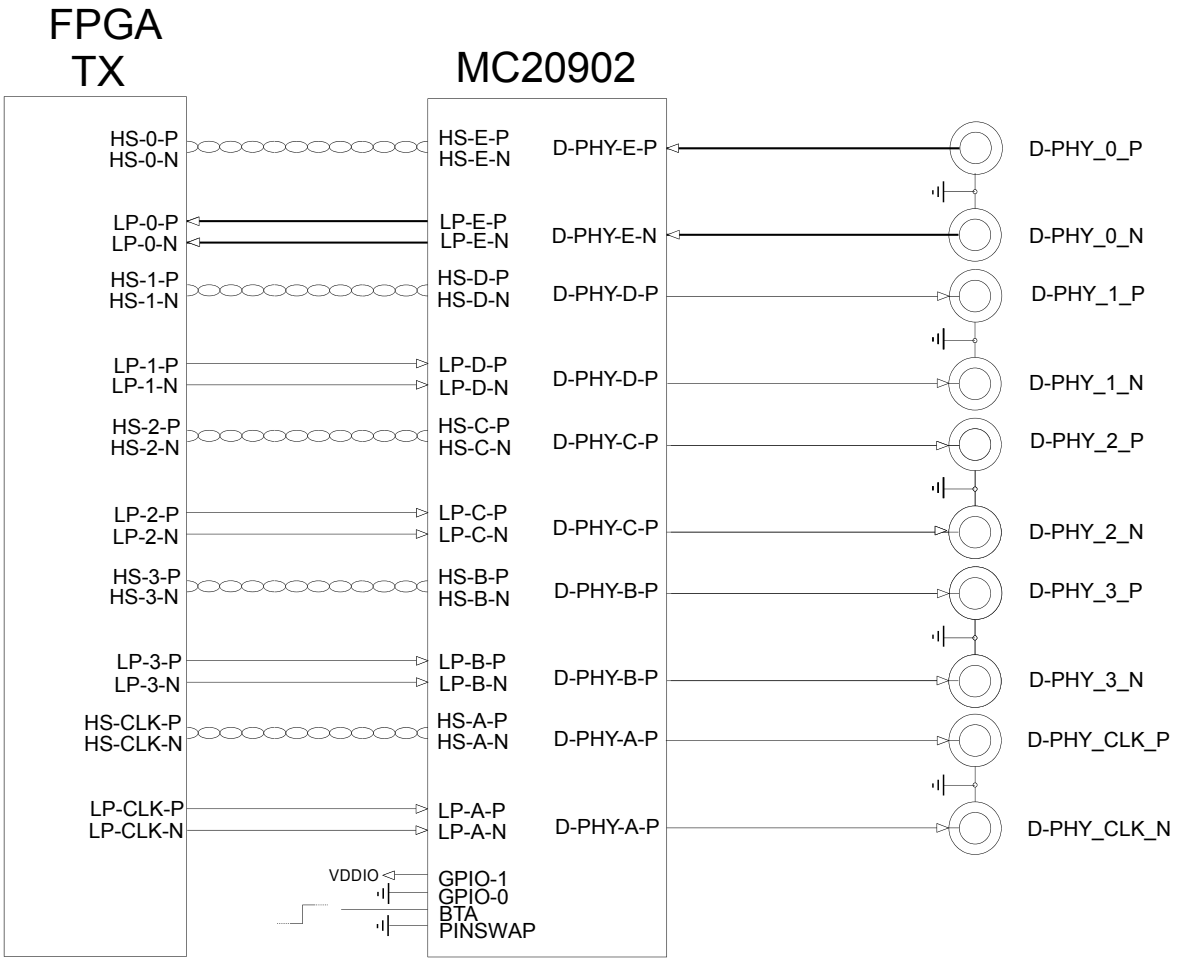


Figure 6: FPGA to D-PHY Bridge Application

6.3 FPGA to D-PHY Bridge Application with Bus Turnaround

In this example one D-PHY clock lane and four D-PHY data lanes are shown.
The setting for Bus Turnaround on Channel E is shown in the Figure 7 below.



Channels A … E are arbitrary exchangeable
Configuration shown is for Bus Turnaround on Channel E.

Figure 7: FPGA to D-PHY Bridge Application with Bus Turnaround (see 6.6)

6.4 Signal Levels

6.4.1 HS-X-P and HS-X-N LVDS Inputs *)

The allowed common mode range is between 700mV and 1.6 Volt for DC coupling.
The inputs can also be AC coupled.

6.4.2 LP-X-P and LP-X-N CMOS Inputs *)

The signals are in the VDDIO domain.

6.4.3 D-PHY-X-P and D-PHY-X-N Outputs *)

These signals are compliant with the MIPI D-PHY specification.

6.4.4 GPIO-0, GPIO-1, BTA, PINSWAP CMOS inputs

The signals are in the VDDIO domain.

*) X means the Channels A to E

6.5 Configuration Using GPIO-0 and GPIO-1

GPIO-1	GPIO-0	Description	
0	0	IC Power Down	
0	1	LVDS to SLVS Level shift	
1	0	D-PHY mode, Bus Turnaround capability assigned to channel E	
1	1	D-PHY mode, Bus Turnaround capability assigned to channel A	

Table 6: GPIO Selection Bits in MIPI D-PHY Mode

6.6 Configuration Using BTA

BTA	Description	
0	Bus Turnaround not enabled	
1	Bus Turnaround enabled on the channel selected according to Table 6. The direction of the LP data transmission is changing instantaneously.	

Table 7: BTA Selection Bits

A low level at BTA Pin means that the LP Pins are treated as input pins (normal operation).
A high level at the BTA Pin means that the LP Pins for the selected channel (see Table 6) are acting as output pins. In this configuration the incoming LP signals on the selected D-PHY-X-P and D-PHY-X-N pins are outputted at the corresponding LP pins LP-X-P and LP-X-N.

6.7 Configuration Using PINSWAP

PINSWAP	Description	
0	Pin Swap off	
1	Pin Swap D-PHY-X (swaps D-PHY-X-P and D-PHY-X-N pins)	
floating	Pin Swap HS-X (swaps HS-X-P and HS-X-N pins)	

Table 8: PINSWAP Selection Bits

6.8 Input to Output Signal Diagram

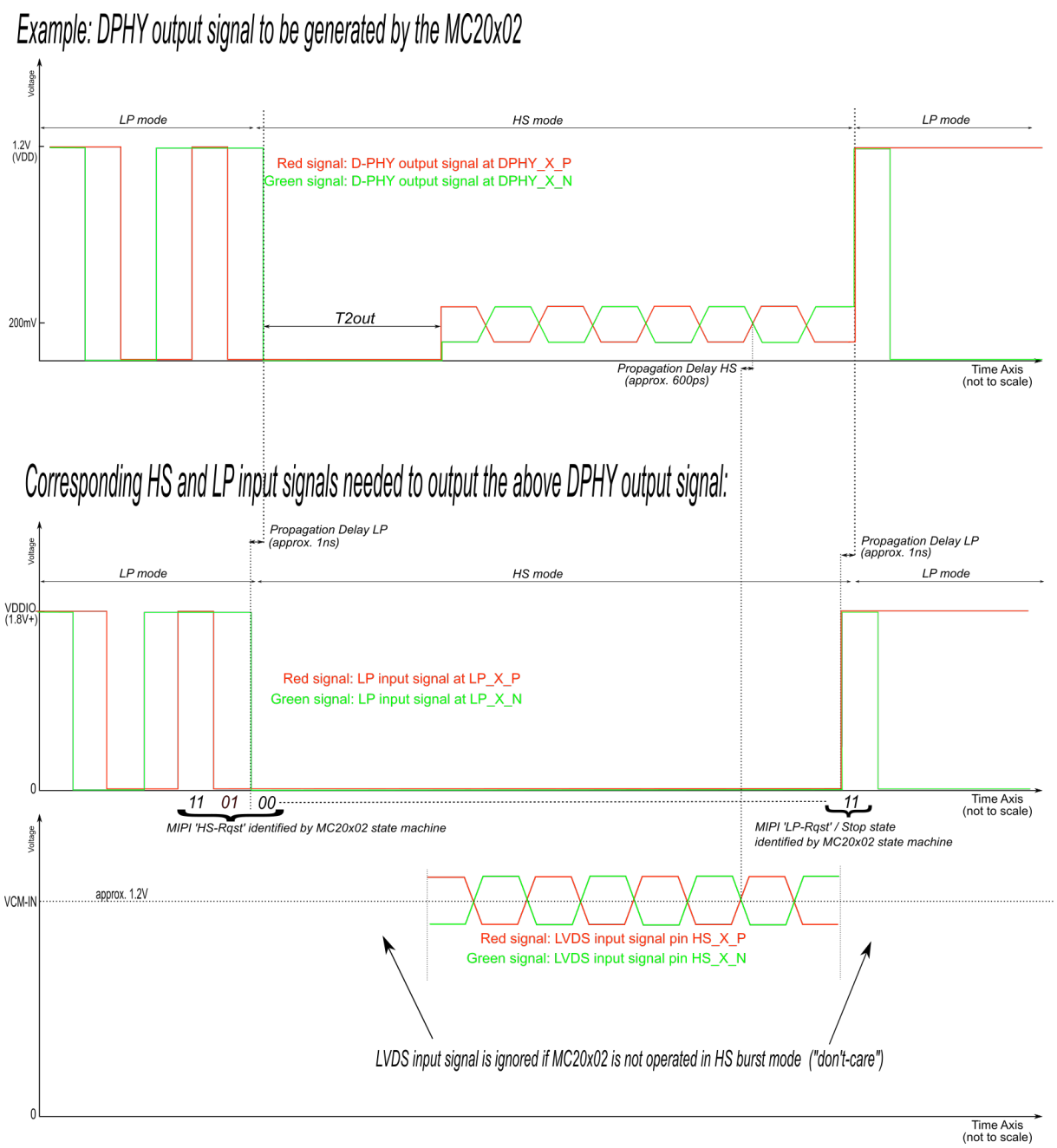


Figure 8: Input to Output Signal Diagram

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